memory addresses without requiring expensive multiply or divide operations. A block of unused sequential addresses in memory space can be allocated to define the phantom port, as described in the specification. Therefore, the use of the phantom port as claimed facilitates performance improvements without requiring additional hardware.

By contrast, the cited reference neither teaches nor discloses the elements of claim 1. Nishide merely discloses a system for improving line drawing performance by detecting horizontal line segments and performing block transfers corresponding to the detected horizontal line segments. Nishide neither hints nor suggests the use of a phantom port to perform remapping as claimed herein.

Nishide's description of address translation (at col. 5, lines 37-50) merely describes translating an X-Y address to a linear address (physical address) for memory access by using segmentation or the like. There is no mention of a phantom port or of a phantom port address as claimed herein. In fact, the Paging (TLB) block of Nishide's Figure 2 is merely described as supporting "a virtual memory mechanism as that of the CPU 1", but with no hint or suggestion of a phantom port. Without the steps of defining a phantom port, generating an address to the phantom port, and determining an address corresponding to the generated phantom port address, as claimed herein, Nishide is not able to provide the distinct advantages of Applicant's invention.

Claims 2 through 5 are dependent upon claim 1, and incorporate all of the limitations of claim 1, including those that distinguish the claims from the Nishide reference. Claims 2 through 5 further recite additional limitations. In particular the limitation of claim 4 that "the phantom port has a span size equal to a power of two" provides further performance advantages

by allowing remapping operations to be implemented using simple field extraction and bit shifting, as described in the specification. Claim 5 recites a further limitation that "c) comprises determining an address in memory address space by extracting at least one field from the phantom port address." The determination of a memory address is thus performed in a highly efficient manner by simple extraction of a field, thereby further improving performance. Applicant respectfully submits that such limitations are not suggested nor made obvious by the disclosure of Nishide.

Claim 6 recites:

> "A computer-implemented method for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, the method comprising the steps of:
>
> a) determining a span of first coordinates of pixels of the display panel;
> b) defining a virtual frame buffer having a first dimension at least as large as the span of the first coordinates;
> c) generating a virtual address indicating a first coordinate and second coordinate of a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel, with the virtual address identifying a memory cell; and
> d) performing one of a reading operation and a writing operation of a representation of the pixel in the memory cell identified by the virtual address."

Claim 14 recites:

> "A computer-implemented method for accessing representations of pixels of a display panel in a frame buffer, the display panel having a plurality of pixels each pixel having a first coordinate and a second coordinate, the method comprising the steps of:
>
> a) determining a span of first coordinates of pixels of the display panel;
> b) selecting a second tile span representing a length of a tile of the display panel along the second coordinates of pixels of the display panel;
> c) defining a virtual frame buffer having a first dimension at least as large as the span of the first coordinates times the second tile span;
> d) generating a virtual address indicating a first coordinate and a second coordinate for a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel; and
> e) performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell of the frame buffer identified by the virtual address."

The claimed method thus employs a virtual frame buffer to provide rapid addressing of video data. A virtual address for a pixel can be rapidly

generated by the present invention using shifting, replacing, or concatenation operations applied to received coordinates of a pixel without the need for the complicated and relatively slow arithmetic hardware. The present invention can access the frame buffer quickly using the virtual address for reading or writing video data in the associated memory cell of the frame buffer. Expensive multiply and divide operations are avoided in favor of concatenation, shifting, and simple field extraction, as described in the specification.

By contrast, Nishide neither teaches nor discloses the elements of claims 6 and 14. As discussed above, Nishide merely discloses a system for improving line drawing performance by detecting horizontal line segments and performing block transfers corresponding to the detected horizontal line segments. The address translation buffer (TLB) disclosed at col. 5, line 48 is used merely to perform address translation by paging; there is no description of any use of a virtual frame buffer and virtual addresses as recited in claims 6 and 14 herein.

Claims 7 through 13 are dependent upon claim 6, and incorporate all of the limitations of claim 6, including those that distinguish the claims from the Nishide reference. Claims 15 through 17 and 19 through 21 are dependent upon claim 14, and incorporate all of the limitations of claim 14, including those that distinguish the claims from the Nishide reference. Claims 7-13, 15-17, and 19-21 further recite additional limitations. In particular, claims 8 and 16 recite "defining a base value, and wherein the first dimension of the virtual frame buffer is a power of the base value." This provides additional performance benefits by allowing remapping to occur using simple shifting and extraction operations. Claim 10 recites "concatenating the bit representation of the first coordinate of the pixel to the bit representation of the second coordinate of the pixel." The recited limitation thus provides another technique

for improving performance in remapping using simple concatenation operations and avoiding expensive addition or multiplication operations. Applicant respectfully submits that such limitations are not suggested nor made obvious by the disclosure of Nishide, which merely mentions address translation using paging.

Claim 22 recites:

> "A system for remapping between pixel coordinate space and memory address space, comprising:
>
> a central processing unit;
>
> a frame buffer memory coupled to the central processing unit and having an associated memory address scheme;
>
> a memory address device coupled to the central processing unit for defining a phantom port containing a plurality of memory addresses, each of a subset of the memory addresses mapping to an address in the frame buffer memory; and
>
> a remapping device coupled to the memory address device for converting an address between the memory address scheme of the frame buffer memory and a memory address of the phantom port."

The claimed system thus provides an apparatus for remapping between pixel coordinate space and memory address space, and thereby facilitating an improvement in the speed of access to a frame buffer. The claimed system includes a memory address device for defining a phantom port, and a remapping device which performs remapping among coordinates and memory addresses without requiring expensive multiply or divide operations. A block of unused sequential addresses in memory space can be allocated to define the phantom port, as described in the specification. Therefore, the use of the phantom port as claimed facilitates performance improvements without requiring additional hardware.

By contrast, the cited reference neither teaches nor discloses the elements of claim 22. As discussed above, Nishide merely discloses a system for improving line drawing performance by detecting horizontal line segments and performing block transfers corresponding to the detected horizontal line

segments. Nishide neither hints nor suggests the use of a phantom port and remapping device to perform remapping as claimed herein.

Nishide's description of address translation (at col. 5, lines 37-50) merely describes translating an X-Y address to a linear address (physical address) for memory access by using segmentation or the like. There is no mention of a phantom port or remapping device as claimed herein. In fact, the Paging (TLB) block of Nishide's Figure 2 is merely described as supporting "a virtual memory mechanism as that of the CPU 1", but with no hint or suggestion of a phantom port. Without including a memory address device for defining a phantom port, and a remapping device for converting addresses as claimed herein, Nishide is not able to provide the distinct advantages of Applicant's invention.

Claim 23 is dependent upon claim 22, and incorporates all of the limitations of claim 22, including those that distinguish the claims from the Nishide reference. Claim 23 further recites that "the defined phantom port has a span equal in size to a power of two, and wherein the remapping device comprises at least one field extractor for extracting fields from the memory address of the phantom port." This additional limitation provides further performance advantages by allowing remapping operations to be implemented using simple field extraction and bit shifting, as described in the specification. Applicant respectfully submits that such limitations are not suggested nor made obvious by the disclosure of Nishide.

Claim 24 recites:

> "A system for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, comprising:
> a processing unit;
> a data accessing module for converting pixel coordinates to virtual frame buffer addresses;
> a video controller for transmitting video data;
> a system memory including a frame buffer for storing digital video data;

a bus coupled to the processing unit, the data accessing module, the video controller, and the system memory, for transmitting data therebetween; and

a display system coupled to the video controller for receiving and displaying video data on the display panel."

The claimed system thus provides functionality for converting pixel coordinates to virtual frame buffer addresses so that representations of pixels for a display panel can be accessed. The claimed system can therefore be used in conjunction with a virtual frame buffer as described previously, in order to provide improved performance in pixel accessing operations.

By contrast, Nishide neither teaches nor discloses the elements of claim 24, and in particular fails to disclose any elements for converting pixel coordinates to virtual frame buffer addresses. As discussed above, Nishide merely discloses a system for improving line drawing performance by detecting horizontal line segments and performing block transfers corresponding to the detected horizontal line segments. The address translation buffer (TLB) disclosed at col. 5, line 48 is used merely to perform address translation by paging; there is no description of any use of a virtual frame buffer as claimed herein.

Claims 25 through 29 are dependent upon claim 24, and incorporate all of the limitations of claim 24, including those that distinguish the claims from the Nishide reference. Claims 25 through 29 further recite additional limitations. In particular, claim 26 recites that "the virtual frame buffer addresses are arranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses using concatenation." Claim 27 recites that "the first and second coordinates of the pixel are stored as bit representations and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses by concatenating the bit representation of the

first coordinate of the pixel to the bit representation of the second coordinate of the pixel." These limitations facilitate improved performance by allowing pixel coordinates to be converted using simple concatenation, without the need for more complex mathematical operations. Claim 29 recites that "the virtual frame buffer addresses are arranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts virtual frame buffer addresses to pixel coordinates using bit field extraction." This limitation facilitates improved performance by allowing pixel coordinates to be converted using simple bit field extraction. Applicant respectfully submits that such limitations are not suggested nor made obvious by the disclosure of Nishide, which merely mentions address translation using paging.

The Examiner objected to claim 18, but indicated that claim 18 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Claim 18 has been so amended.

Claims 7 and 8 have been amended merely to correct minor typographical errors.

Accordingly, Applicants respectfully submit that claims 1-29 are patentable over the cited art.

No additional fee is due. The application now contains six independent claims. Six independent claims were paid for at the time of filing.

On the basis of the above amendments and remarks, consideration of this application and the early allowance of all claims herein are requested.

Favorable action is solicited.

Respectfully submitted,

ROGER W. SWANSON

Dated: JAN 6/99 By: _____

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